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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,849	01/22/2004	Mark A. Horowitz	60809-5000	8501

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EXAMINER	
AUVE, GLENN ALLEN	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 09/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/763,849	HOROWITZ ET AL.	
	Examiner	Art Unit	
	Glenn A. Auve	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *32-73* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *59-66* is/are allowed.

6)☒ Claim(s) *32-34,36-38,40-45,48-50,52-56,67,68 and 70-72* is/are rejected.

7)☒ Claim(s) *35,39,46,47,51,57,58,69 and 73* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1-10 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance. The specification indicates that figures 1 and 2 are prior bus systems and figures 3-10 appear to be related to the systems shown in figures 1 and 2, therefore they also appear to be prior art. The drawings should be corrected in order to indicate clearly what is prior art and what is not prior art.

Claim Objections

2. Claim 58 is objected to because of the following informalities: in claim 58, line 1, "storing a n additional value" should be corrected, probably to "storing an additional value". Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 32-34,36-38,40-45,48-50,52-56,67,68, and 70-72 are rejected under 35 U.S.C. 102(e) as being anticipated by Barth et al., U.S. Pat. No. 6,154,821.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As per claim 32, Barth et al. (Barth) shows a memory system, comprising: a memory module (100) including: a plurality of memory devices (110,112,114,116) disposed on the memory module; a supplemental memory device that stores information pertaining to the plurality of memory devices disposed on the memory module (col.7, lines 15-30); and an integrated circuit device (102) having controller circuitry that communicates with the plurality memory of devices, the integrated circuit device including: a receiver circuit to sample receive data from an external signal line at a sample time (140); and a first register to store a first value representative of a sampling time adjustment (150) that is applied to the sample time, wherein the first value is determined based on the information pertaining to the plurality of memory devices (col.7). Barth shows all of the elements recited in claim 32.

As for claim 33, the argument for claim 32 applies. Barth also shows that the sample time is indicated by an internal receive signal, wherein the internal receive signal is adjusted, based on the first value, to apply the sampling time adjustment to the sample time (cols. 5 and

7, wherein the receive sampling time for the memory devices is adjusted for each device). Barth shows all of the elements recited in claim 33.

As for claim 34, the argument for claim 33 applies. Barth also shows a locked loop circuit to generate the internal receive signal (154). Barth shows all of the elements recited in claim 34.

As for claim 36, the argument for claim 32 applies. Barth also shows that the information pertaining to the plurality of memory devices is determined by accessing the supplemental memory device (col.7). Barth shows all of the elements recited in claim 36.

As for claim 37, the argument for claim 36 applies. Barth also shows that the supplemental memory device is a serial presence detect memory device (col.7). Barth shows all of the elements recited in claim 37.

As for claim 38, the argument for claim 32 applies. Barth also shows a delay locked loop circuit (154) to generate an internal receive signal, wherein a phase of the internal receive signal is adjusted, based on the first value, to apply the sampling time adjustment to the sample time (cols. 5 and 8). Barth shows all of the elements recited in claim 38.

As for claim 40, the argument for claim 32 applies. Barth also shows that the sampling time adjustment is a predetermined phase offset that is based on the first value (cols. 5 and 7). Barth shows all of the elements recited in claim 40.

As for claim 41, the argument for claim 32 applies. Barth also shows that the information pertaining to the plurality of memory devices includes a number of memory devices included in the memory system (col.7). Barth shows all of the elements recited in claim 41.

As for claim 42, the argument for claim 32 applies. Barth also shows that the integrated circuit device is a dynamic random access memory device (at least in the abstract). Barth shows all of the elements recited in claim 42.

As for claim 43, the argument for claim 32 applies. Barth also shows that the integrated circuit device is a microprocessor device (the memory controller 102 is a processor of data and signals). Barth shows all of the elements recited in claim 43.

As for claim 44, the argument for claim 32 applies. Barth also shows a transmitter circuit to transmit transmit data in response to an internal transmit signal (140); and a second register (152) to store a second value representative of a transmit time adjustment that is applied to the internal transmit signal, wherein the second value is determined based on the information pertaining to the plurality of memory devices (cols. 5 and 7). Barth shows all of the elements recited in claim 44.

As for claim 45, the argument for claim 44 applies. Barth also shows a third register to store a third value representative of a slew rate adjustment that is applied to the transmitter circuit (col.7). Barth shows all of the elements recited in claim 45.

As per claim 48, Barth shows a method of operation in a memory system, wherein the memory system includes an integrated circuit controller device that communicates with a plurality of memory devices, the method comprising: reading information from a supplemental memory device that pertains to the plurality of memory devices (col.7); determining a first value that represents a sample time adjustment to apply to a sample time of a receiver circuit in the integrated circuit controller device, wherein the sample time adjustment is based on the information from the supplemental memory device (col.5); and storing the first value in a first register on the integrated circuit controller device (col.5). Barth shows all of the steps recited in claim 48.

As for claim 49, the argument for claim 48 applies. Barth also shows that the sample time is indicated by an internal receive signal, wherein the method further includes adjusting the

internal receive signal based on the first value to apply the sampling time adjustment to the sample time (col.5). Barth shows all of the steps recited in claim 49.

As for claim 50, the argument for claim 49 applies. Barth also shows generating the internal receive signal using a locked loop circuit, and wherein adjusting the internal receive signal further includes modifying a circuit element of the locked loop circuit (cols. 5 and 8). Barth shows all of the steps recited in claim 50.

As for claim 52, the argument for claim 49 applies. Barth also shows that the sampling time adjustment is applied to the sample time by introducing a phase offset to a phase of the internal receive signal (cols. 5 and 8). Barth shows all of the steps recited in claim 52.

As for claim 53, the argument for claim 48 applies. Barth also shows that the supplemental memory device is a serial presence detect memory device (col.7). Barth shows all of the steps recited in claim 53.

As for claim 54, the argument for claim 48 applies. Barth also shows that the integrated circuit controller device is a microprocessor device (the memory controller 102 is a processor of data and signals). Barth shows all of the steps recited in claim 54.

As for claim 55, the argument for claim 48 applies. Barth also shows transmitting transmit data from the integrated circuit controller device to at least one memory device of the plurality of memory devices, in response to an internal transmit signal; and storing a second value representative of a transmit time adjustment that is applied to the internal transmit signal, wherein the second value is determined based on the information from the supplemental memory device (cols. 5 and 7). Barth shows all of the steps recited in claim 55.

As for claim 56, the argument for claim 55 applies. Barth also shows storing a third value that is representative of a slew rate adjustment that is applied to the transmitter circuit (col.7). Barth shows all of the steps recited in claim 56.

As per claim 67 Barth shows a memory system, comprising: a plurality of dynamic random access memory devices (110,112,114,116); and an integrated circuit controller device (102) that communicates with the plurality of dynamic random access memory devices, the integrated circuit controller device including: a receiver circuit (140) to sample receive data from an external signal line at a sample time that is indicated by an internal receive signal; and a first register (150) to store a first value representative of a sampling time adjustment that is applied to the sample time by adjusting a phase of the internal receive signal, wherein the first value is determined based on information stored in a serial presence detect memory device (cols. 5 and 7). Barth shows all of the elements recited in claim 67.

As for claim 68, the argument for claim 67 applies. Barth also shows a locked loop circuit to generate the internal receive signal (154). Barth shows all of the elements recited in claim 68.

As for claim 70, the argument for claim 67 applies. Barth also shows that a serial presence detect memory device is disposed on a memory module substrate along with the plurality of dynamic random access memory devices (col.7). Barth shows all of the elements recited in claim 70.

As per claim 71 Barth shows a memory system, comprising: a plurality of dynamic random access memory devices (110,112,114,116); and an integrated circuit controller device (102) that communicates with the plurality of dynamic random access memory devices, the integrated circuit controller device including: a means for sampling receive data from an external signal line at a sample time that is indicated by an internal receive signal (140); and a means for storing a first value representative of a sampling time adjustment (150) that is applied to the sample time by adjusting a phase of the internal receive signal, wherein the first value is determined based on information stored in a serial presence detect memory device (col.7). Barth shows all of the elements recited in claim 71.

As for claim 72, the argument for claim 71 applies. Barth also shows a locked loop circuit to generate the internal receive signal (154). Barth shows all of the elements recited in claim 72.

Allowable Subject Matter

5. Claims 35,39,46,47,51,57,58,69, and 73 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 59-66 are allowed.

7. The following is a statement of reasons for the indication of allowable subject matter: with respect to claims 35,51,59,69, and 73, the prior art does not appear to specifically show that the sample time is adjusted to substantially center a data eye of the receive data with respect to the internal receive signal.

8. With respect to claim 39, the prior art does not show the use of a phase locked loop in combination with the other elements recited in the claim.

9. With respect to claims 46 and 57, the prior art does not show a third register to store a third value representative of a drive strength adjustment that is applied to the transmitter circuit.

10. With respect to claims 47 and 58, the prior art does not show storing an additional value representative of a reference voltage level adjustment that is applied to a reference voltage to derive a modified reference voltage level, and sampling in the receiver circuit of the integrated circuit controller device receive data using the modified voltage reference level.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn A. Auve whose telephone number is (571) 272-3623. The examiner can normally be reached on M-F 8:00 AM-5:30 PM, every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Glenn A. Auve
Primary Examiner
Art Unit 2111

gaa
13 September 2005